2, it will be recalled that each controller has a dedicated packet bus for transmitting data bursts to all controllers simultaneously. Receive ports 701-709 perform filtering checks and, where indicated, stalling checks on received packets and are assigned distinct "start release" clock cycles within a repetitive timing cycle such that, if both the filtering and stalling checks are passed, receive ports 701-709 may initiate the release of packets to forwarding queue 720 on their assigned "start release" clock cycles. Packets in forwarding queue 720 are eventually forwarded to LAN port controller 510 for a VLAN check and, where indicated, transmission on protocol domains 540. Receive ports 701-709, of course, have associated claim lines 311-319 and stall lines 411-419 for employing, where indicated, in the preferred filtering and stalling systems.

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REMARKS

Claims 1-3 and 9-13 are now pending in this application.

The specification and FIG. 8 of the drawings have been amended to correct inconsistencies in the reference numbering. Applicant respectfully requests entry of these amendments.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Haddock (U.S. Patent No. 6,023,471). Claims 1-2 and 12 are also rejected under 35 U.S.C. 102(e) as being anticipated by Perlman. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman in view of Shimizu (U.S. Patent No. 4,866,702). Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perlman in view of Scoot (U.S. Patent No. 5,953,340) and Shimizu.

The Haddock reference claims priority of a provisional application filed on October 7, 1997. The Perlman reference is a continuation of an application filed on January 7, 1997. The Shimizu reference was filed on September 21, 1988. However, Applicant invented the claimed invention and reduced it to practice prior to January 7, 1997, as set forth in the accompanying Rule 131

declaration. Applicant has therefore antedated the Haddock, Perlman, and Shimizu references, and obviated the rejections.

In view of the foregoing remarks, Applicant respectfully requests an early indication of allowance of claims 1-3 and 9-13.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Also submitted herewith is amended FIG. 8 along with a REQUEST FOR APPROVAL OF DRAWING CHANGE. It is requested that the drawing change be reviewed and approved by the Examiner. Applicant will formalize the drawing after allowance of the application.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By _____
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626/795-9900

JEC/daa

"Version with markings to show changes made"

In the Specification:

The paragraph starting on page 9, line 8 to the first paragraph on page 12 have been amended as follows:

Turning now to Figure 5, switching controller [~~201~~] 500 operative on LAN switch backplane 200 is shown. Switching controller [~~201~~] 500 is representative of switching controllers 201-208 and is also representative of the switching elements of management controller 209. However, management controller 209 has other elements for assisting source learning. Accordingly, management controller 209 may be regarded as an enhanced switching controller. Controller [~~201~~] 500 includes LAN port controller 510 and receive interface 520 sharing filtering logic 530. LAN port controller 510 captures packets off protocol domains 540, formats them and propagates them on dedicated packet bus 211 as the root controller for that bus. Subject to filtering rules, receive interface 520 captures packets off packet buses 211-219 as one of the leaf controllers for that bus, formats them and forwards them to LAN port controller 510. Subject to VLAN rules, LAN port controller 510 receives packets from receive interface 520, formats them and propagates them on protocol domains 540. Although a plurality of protocol domains are illustrated, controller [~~201~~] 500 may be associated with one or more protocol domains, as network requirements demand. Transmit and receive processing are preferably performed on controller [~~201~~] 500 using direct memory access (DMA) techniques implemented in integrated circuitry, although processor intervention is judiciously employed for configuration and relatively high-level tasks. Protocol domains 540 preferably each include one or more network devices operating in a particular communication protocol, such as Ethernet (operating at 10 Mbps, 10/100 Mbps, 100 Mbps or 1000 Mbps), Token Ring FDDI or ATM. Naturally, if the operative protocol is ATM, controller 500, in addition to the

functionality described herein, has segmentation and reassembly (SAR) logic to accomplish packet-to-cell and cell-to-packet conversions. It bears noting that the plurality of controllers 201-209 sharing backplane 200 at the same time may support protocol domains operative in disparate communication protocols. Thus, for example, one of controllers 201-209 may support Fast Ethernet protocol domains, while a second may support Token Ring protocol domains, and a third may support an ATM protocol domain.

Turning now to Figure 6, filtering logic 530 operative on representative switching controller [~~201~~] 500 will be described in greater detail. Logic 530 is dual-ported for shared access by LAN port controller 510 and receive interface 520. Memory 630 may be accessed via transmit filter control 610 and receive filter control 620, associated with LAN port controller 510 and receive interfaces 520, respectively. Memory 630 includes a CAM 632 having entries holding, at different CAM indices, learned forwarding addresses of network devices residing on the controller's protocol domains. Forwarding addresses also may include configured flood addresses for forwarding broadcast packets. Memory 630 also includes CAM associated data 634 having entries linked to entries in CAM 632 or in the CAM on another one of controllers 202-209 by a common CAM index. CAM associated data entries include a flood field, a "last seen" field, a VLAN field and a port field. The flood field holds a flag indicating whether the entry is associated with a flood address. The "last seen" field holds a time stamp indicating the last time the entry was accessed. The VLAN field identifies the VLAN membership of the network device, if any, to which the entry relates. The VLAN field may include multi-bit numerical represenations for each identified VLAN or may be in the form of a VLAN mask in which a VLAN is identified by the bit value retained at a position in the entry reserved for the VLAN. The port field identifies the number of the LAN port through which the network device to which the entry relates, if any, accesses controller [~~201~~] 500. As is well known, addresses

submitted to CAM 632 return, in a single "look-up" operation, all indices at which a matching address resides. The returned indices may be advantageously used to consult the corresponding entry in CAM associated data 634 and retrieve information associated with the matching address. Of course, other types of memory elements and logic may be implemented in lieu of CAM 632, such as a "pseudo CAM" which resolves the most distinctive bits in addresses using a data hashing algorithm and conducts associative comparisons in a random access memory (RAM) using the most distinctive bits. CAM associated data 634 may be implemented in RAM.

Referring now to Figure 7, receive interface 520 operative on representative controller [~~201~~] 500 is shown in greater detail. Receive interface 520 implements preferred filtering and stalling systems with the expedients of receive ports 701-709, receive filter control 620, watermark checker 710 and forwarding queue 720. Each receive port has a receive buffer fed with data bursts arriving off a different one of packet buses 211-219. In this regard, returning momentarily to Figure 2, it will be recalled that each controller has a dedicated packet bus for transmitting data bursts to all controllers simultaneously. Receive ports 701-709 perform filtering checks and, where indicated, stalling checks on received packets and are assigned distinct "start release" clock cycles within a repetitive timing cycle such that, if both the filtering and stalling checks are passed, receive ports 701-709 may initiate the release of packets to forwarding queue 720 on their assigned "start release" clock cycles. Packets in forwarding queue 720 are eventually forwarded to LAN port controller 510 for a VLAN check and, where indicated, transmission on protocol domains 540. Receive ports 701-709, of course, have associated claim lines 311-319 and stall lines 411-419 for employing, where indicated, in the preferred filtering and stalling systems.